16-CH LEVEL SHIFTER FOR GOA TFT-LCD PANEL

FEATURES

- 2.6V to 5.5V Input Logic Level Range
- -18V to 40V Output Voltage Range
- 16 Ch Level Shifter Support 10-CH CLK, 2-CH STV, LC1/2, DIS_VGL, DIS_LVGL
- CLK_IN1/2, STV_IN1/2, LC_IN, Terminate, DIS_SENSE, A0 inputs
- FAULT output
- VDD, VGH, LVGL, VGL power pins
- Protection Functions: UVLO, OTP, OCP
- Support 2-In Multi-Out
- I2C Interface, Slave Address 50h/52h
- Power Off Discharge Option
- 2-Line Mode
- RoHS Compliant and Halogen Free

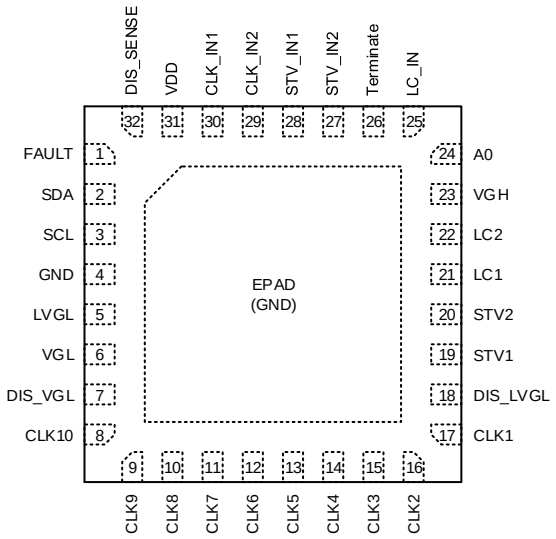
GENERAL DESCRIPTION

The iML7272A is a high voltage level shifter. This device is suitable for GOA TFT-LCD panel applications. The level shifter is designed for generating a high voltage signal to drive the TFT-LCD panel. Sixteen outputs are provided to switch between LVGL/VGL and VGH to charge and discharge capacitive loads of up to 5nF.

APPLICATIONS

- GOA TFT-LCD Panel

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE TYPE	PART NUMBER	PACKAGE	PACKING	TEMP. RANGE	MARKING	MARKING DESCRIPTION
iML7272A	iML7272AID-TR	ID: QFN32-4X4	Tape And Reel	–40°C to +85°C	i7272A XYYWWZZZ	i7272A: Part Name YYWW: Date code XZZZ: Lot No.

Note: All CHIPONE products are lead free and halogen free.

TYPICAL APPLICATION

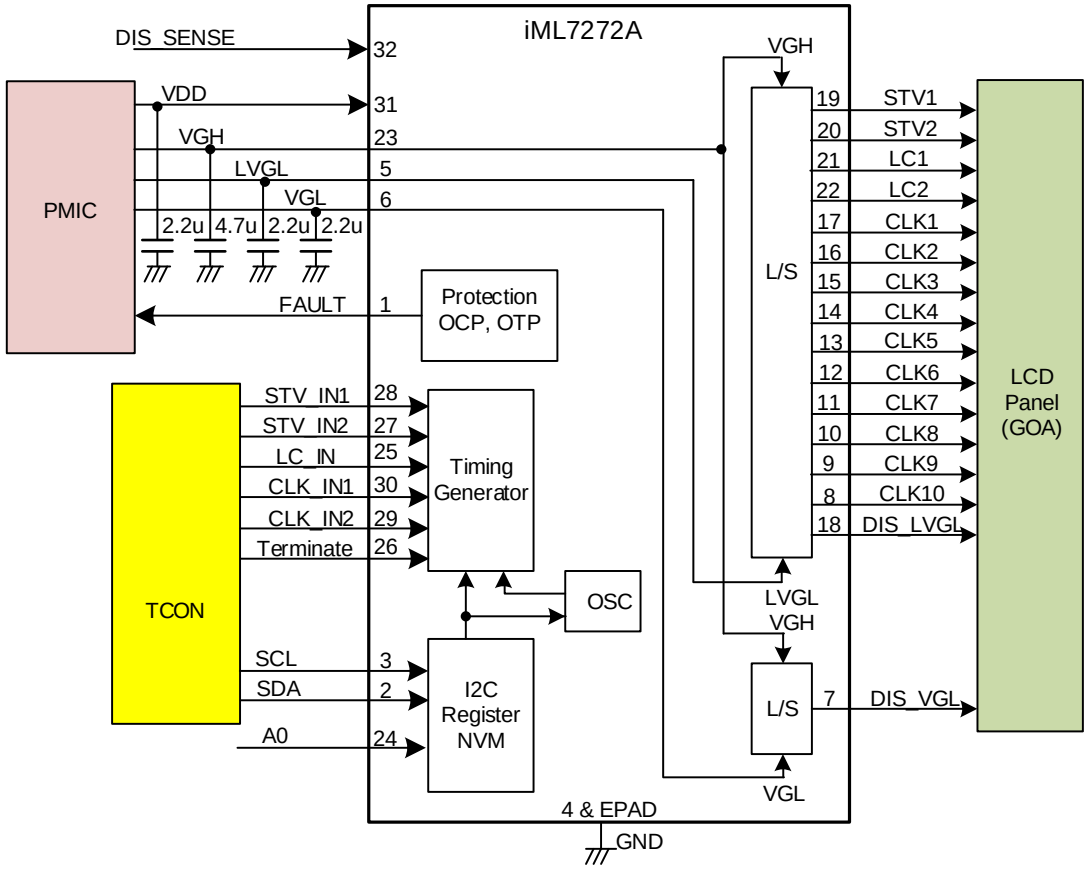


Figure 1. The iML7272A Application Circuit

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Parameters	Symbol	Value	Units
Supply Input Voltag, VDD (continuous)	V_{IN}	-0.3 to +7	V
Ground Voltage	V_{IN2}	-0.3 to +0.3	V
STV_IN1, STV_IN2, LC_IN, CLK_IN1, CLK_IN2, TERMINATE to GND	V_{H1}	-0.3 to +7	V
DIS_SENSE, A0 to GND	V_{H2}	-0.3 to +7	V
VGH to GND	V_{H3}	-0.3 to +45	V
FAULT to GND	V_{H4}	-0.3 to +10	V
VGL, LVGL to GND	V_{L1}	-20 to +0.3	V
VGH to [VGL or LVGL]	V_{L2}	-0.3 to +60	V
STV1, STV2, LC1, LC2, [CLK1 to CLK10], DIS_VGL, DIS_LVGL to GND	V_{L3}	(VGL + 0.3V) to (VGH - 0.3V)	V
Power Dissipation, @ T_A = +25°C , T_J = +125°C	P_D	1.84	W
Package Thermal Resistance (Note 2)	θ_{JA}	54.3	℃/W
Package Thermal Resistance (Note 2)	θ_{JC}	6	℃/W
Storage Temperature Range	$T_{STORAGE}$	–65 to +150	℃

RECOMMENDED OPERATING CONDITIONS

Parameters	Symbol	Value	Units
Ambient Temperature Range (Note 3)	T_A	–40 to +85	℃
Junction Temperature Range (Note 3)	T_J	–40 to +125	℃

Notes:

1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. θ_{JA} is measured under natural convection (still air) at T_A= 25°C with the component mounted on a high effective thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.
3. The device is not guaranteed to function outside its operating conditions.

ELECTRICAL CHARACTERISTICS

VDD=3.3V, VGH=30V, VGL=-6V, LVGL=-10V, GND=0V, TA=+25°C unless otherwise specified

Parameters	Symbol	Test Condition	Min	Typ	Max	Units
Supply Current						
Supply Voltage	VDD		2.6	--	5.5	V
VDD Quiescent Current	I_{Q-VDD}	DIS_SENSE=High	--	0.7	--	mA
VGH Quiescent Current	I_{Q-VGH}	DIS_SENSE=High	--	0.6	--	mA
VGL Quiescent Current	I_{Q-VGL}	DIS_SENSE=High	--	0.15	--	mA
LVGL Quiescent Current	I_{Q-LVGL}	DIS_SENSE=High	--	0.4	--	mA
DIS_SENSE Quiescent Current	I_{Q-DIS_SENSE}	DIS_SENSE=High	--	1	--	uA
Protections						
VDD Under Voltage Lockout Threshold	$V_{UVLO-VDD}$	VDD rising, Hysteresis 200mV	1.95	2.2	2.45	V
		VDD falling	1.75	2.0	2.25	V
VGH Under-Voltage Lockout Threshold	V_{UVLOGH}	VGH rising	14	15	16	V
		VGH falling	4	5	6	V
POR Under-Voltage Lockout Threshold	$V_{UVLOPOR}$	POR falling	--	3.5	--	V
DIS_SENSE Under Voltage Lockout Threshold		DIS_SENSE falling, hysteresis 200mV when Reg03h[5:4]=01	2.37	2.5	2.63	V
Thermal Shutdown	T_{SD}	Junction temperature rising	140	160	180	°C
Thermal Shutdown Hysteresis	T_{SD-HYT}		--	20	--	°C
Internal Pull-Down Resistor (CLK_IN1/2, LC_IN, STV_IN, TERMINATE)			--	400	--	kΩ
A0, FAULT Internal Pull Up Resistor		Pull-up to VDD	--	200	--	kΩ
FAULT Output Low Level	V_{OL}	Current=1mA	-	-	0.4	V
Level Shifter						
VGH to GND	VGH		15	--	40	V
VGL Operating Voltage Range	LVGL	(Note 5)	-18	--	-3	V
LVGL Operating Voltage Range	LVGL	(Note 5)	-18	--	-3	V
CLK_IN1, CLK_IN2, TERMIINATE, STV_IN1, STV_IN2, LC_IN, A0	V_{IH}	VDD = 2.6V to 5.5V	1.5	--	--	V
	V_{IL}	VDD = 2.6V to 5.5V	--	--	0.6	V

CLK_IN1, CLK_IN2,TERMINATE, STV_IN1, STV_IN2 and LC_IN Input Signal Pulse width Signal Pulse Width (Note 6)	V_{IW}	VDD = 2.6V to 5.5V	200	--	--	ns
CLK_IN1/2 Input signal Maximum Frequency			--	--	300	kHz
CLK1 to CLK10, STV1, STV2, LC1 and LC2, Positive Output Swing	V_{CK+}	All inputs high, I_O = 10mA	VGH -0.2	VGH -0.15	VGH	V
CLK1 to CLK10, STV1, STV2, LC1 and LC2, Negative Output Swing	V_{CK-}	All inputs low, I_O = -10mA	LVGL +0.2	LVGL +0.15	LVGL	V
DIS_VGL, DIS_LVGL High-Side Ron			--	25	--	Ω
DIS_VGL, DIS_LVGL Low-Side Ron			--	10	25	Ω
OCP Level for CLK1 to CLK10	OCP1	02h[2:0] = 000	Disable OCP1			-
		02h[2:0] = 001	20	30	40	mA
		02h[2:0] = 010	40	50	60	mA
		02h[2:0] = 011	60	70	80	mA
		02h[2:0] = 100	77	90	103	mA
		02h[2:0] = 101	102	120	138	mA
		02h[2:0] = 110	136	160	184	mA
		02h[2:0] = 111	170	200	230	mA
OCP Level for STV1, STV2, LC1, LC2, DIS_VGL, DIS_LVGL	OCP2	02h[5:3] = 000	Disable OCP2			-
		02h[5:3] = 001	20	30	40	mA
		02h[5:3] = 010	40	50	60	mA
		02h[5:3] = 011	60	70	80	mA
		02h[5:3] = 100	77	90	103	mA
		02h[5:3] = 101	102	120	138	mA
		02h[5:3] = 110 and 111	136	160	184	mA
CLK1 to CLK10, Rising / Falling Slew Rate (Note 7) (Note 8)	t_R	VGH = 30V, LVGL = -10V, R_L = 51ohm, C_L = 4.7nF, 20% to 80%	--	1000	--	V/µs
	t_F	VGH = 30V, LVGL = -10V, R_L = 51ohm, C_L = 4.7nF, 80% to 20%	--	1000	--	V/µs
STV1, STV2, LC1, LC2, Rising / Falling Slew Rate (Note 8)	t_R	VGH = 30V, LVGL = -10V, R_L = 51ohm, C_L = 4.7nF, 20% to 80%	--	300	--	V/µs

	t_F	VGH = 30V, LVGL = -10V, R_L = 51ohm, C_L = 4.7nF, 80% to 20%	--	300	--	V/µs
CLK1 to CLK10, STV1, STV2, LC1, LC2, Rising / Falling Delay Time	t_{RD}	VGH = 30V, LVGL = -10V, 50% of input to 10% of output	--	150	250	ns
	t_{FD}	VGH = 30V, LVGL = -10V, 50% of input to 90% of output	--	150	250	ns
DIS_VGL, DIS_LVGL Rising Time (Note 7)	t_{DIS_LVGL},	VGH = 30V, LVGL = -10V, R_L = 51ohm, C_L = 4.7nF, 10% to 90%	--	--	1	µs
OCP Blank Time for CLK, STV1/2, LC1/2 after transition (Note 9)	Tblk	Error=±20%	2	--	16	µs
OCP Detect Time for CLK, and STV1/2 High-Side	Tsdet	Error=±20%	0		3	µs
OCP Detect time for STV1/2 Low-Side (Note 10)	Tldet		--	40	--	µs
OCP Detect time for LC1/2 High-Side	Tldet		--	40	--	µs
OCP Detect time for LC1/2 Low-Side	Tldet		--	40	--	µs
OCP Detect time for DIS_VGL, DIS_LVGL Low-Side	Tldet		--	40	--	µs
Input Threshold (SCL, SDA)						
Input Low Voltage	V_{IL}		-	-	0.6	V
Input High Voltage	V_{IH}		1.6	-	-	V
I2C Interface						
SCL, SDA Input Capacitance	C_{SI}		-	5	-	pF
SDA Output Low Voltage	V_{OL}	I_{SINK} = 3mA	-	-	0.4	V
SCL Clock Frequency	f_{OSCI2C}		-	-	400k	Hz
SCL Clock High Period	t_{IH3}		0.6	-	-	µs
SCL Clock Low Period	t_{IL3}		1.3	-	-	µs
SCL, SDA Receiving Rise Time	t_{R1}		-	20+0.1*C_B	300	ns
SCL, SDA Receiving Fall Time	t_{F1}		-	20+0.1*C_B	300	ns
I^2C Data Setup Time	t_{S1}		100	-	-	ns
I^2C Data Hold Time	t_{H1}		0	-	900	ns
I^2C Setup Time for START Condition	t_{S2}		0.6	-	-	µs
I^2C Hold Time for START Condition	t_{H2}		0.6	-	-	µs

I²C Bus Free Time Between STOP and START Conditions	t_{BUS}		4.7	-	-	µs
I²C Pulse Width of Suppressed Spike	t_{PS}		0	-	50	ns
I²C Bus Capacitance	C_B		-	-	400	pF
NVM Writing Voltage & Current (Fault)						
NVM writing voltage	V_{Fault}		9.3	9.5	9.7	V
NVM writing current	I_{Fault}		-	1.0	3.0	mA

Notes

5. The sequence of LVGL must be earlier than (or equal to) VGL in application. The voltage of LVGL must be lower than (or equal to) VGL always. If LVGL-VGL>0.3V, abnormal IC function behavior maybe happen.
6. The input signal pulse width must be over 200ns.
7. Rising/Falling time measure point is before RC.
8. CLK1 to CLK10 Slew Rate can select by 03h[7:6].
9. CLK High/Low-Side and STV High-Side Blank time can select by 03h[2:0].
10. For OCP Detect of the Low-Side STV, if one time of OCP condition happens for Tldet(=40us), FAULT is triggered, as similar as LC1/2 cases. The STV_OCP_COUNT does not affect the OCP of Low-Side STV. The STV_OCP_COUNT affects only for the OCP of High-Side STV.

PIN DESCRIPTION

Pin#	Name	I/O	Description
1	FAULT	I/O	FAULT terminal. When NVM writing need to input +9.5V (Refer to Page 26).
2	SDA	I/O	I2C - Compatible serial bidirectional data line
3	SCL	I	I2C - Compatible clock input
4	GND	--	Ground
5	LVGL	P	LC1/2、CLK1 to 10 and STV negative power supply. Refer to function block and application circuit.
6	VGL	P	Low level of DIS_VGL circuit. Please refer to the function and the application circuit
7	DIS_VGL	O	Discharge function for liquid crystal capacitor
8	CLK10	O	Level shifter output.
9	CLK9	O	Level shifter output.
10	CLK8	O	Level shifter output.
11	CLK7	O	Level shifter output.
12	CLK6	O	Level shifter output.
13	CLK5	O	Level shifter output.
14	CLK4	O	Level shifter output.
15	CLK3	O	Level shifter output.
16	CLK2	O	Level shifter output.
17	CLK1	O	Level shifter output.
18	DIS_LVGL	O	Discharge function for liquid crystal capacitor.
19	STV1	O	Level shifter output signal. (Low frequency start pulse 1 for GOA share)
20	STV2	O	Level shifter output signal. (Low frequency start pulse 2 for GOA share)
21	LC1	O	Level shifter output signal. (Low frequency clock 1)
22	LC2	O	Level shifter output signal. (Low frequency clock 2)
23	VGH	P	LC1/2, CLK1 to 10 and STV1/2 positive power supply. Refer to function block and application circuit.
24	A0	I	Slave address assignment
25	LC_IN	I	Level shifter input signal (low frequency clock). The LC is the high/low level trigger.
26	TERMINATE	I	Level shifter input signal. Pull CLK1 to 10 low on TERMINATE rising edge
27	STV_IN2	I	Level Shifter input signal (start pulse for GOA) The STV_IN2 is rising/falling edge trigger.

28	STV_IN1	I	Level Shifter input signal (start pulse for GOA) The STV_IN1 is rising/falling edge trigger.
29	CLK_IN2	I	Level shifter input signal (condensed clock) The CLK_IN2 is rising/falling edge trigger.
30	CLK_IN1	I	Level shifter input signal (condensed clock) The CLK_IN1 is rising/falling edge trigger.
31	VDD	P	Supply voltage input and Level shifter input discharge sensing voltage.
32	DIS_SENSE	I	Level shifter input discharge sensing voltage
33	EP		Exposed Pad. Connect to AGND with copper plane.

POWER SEQUENCE

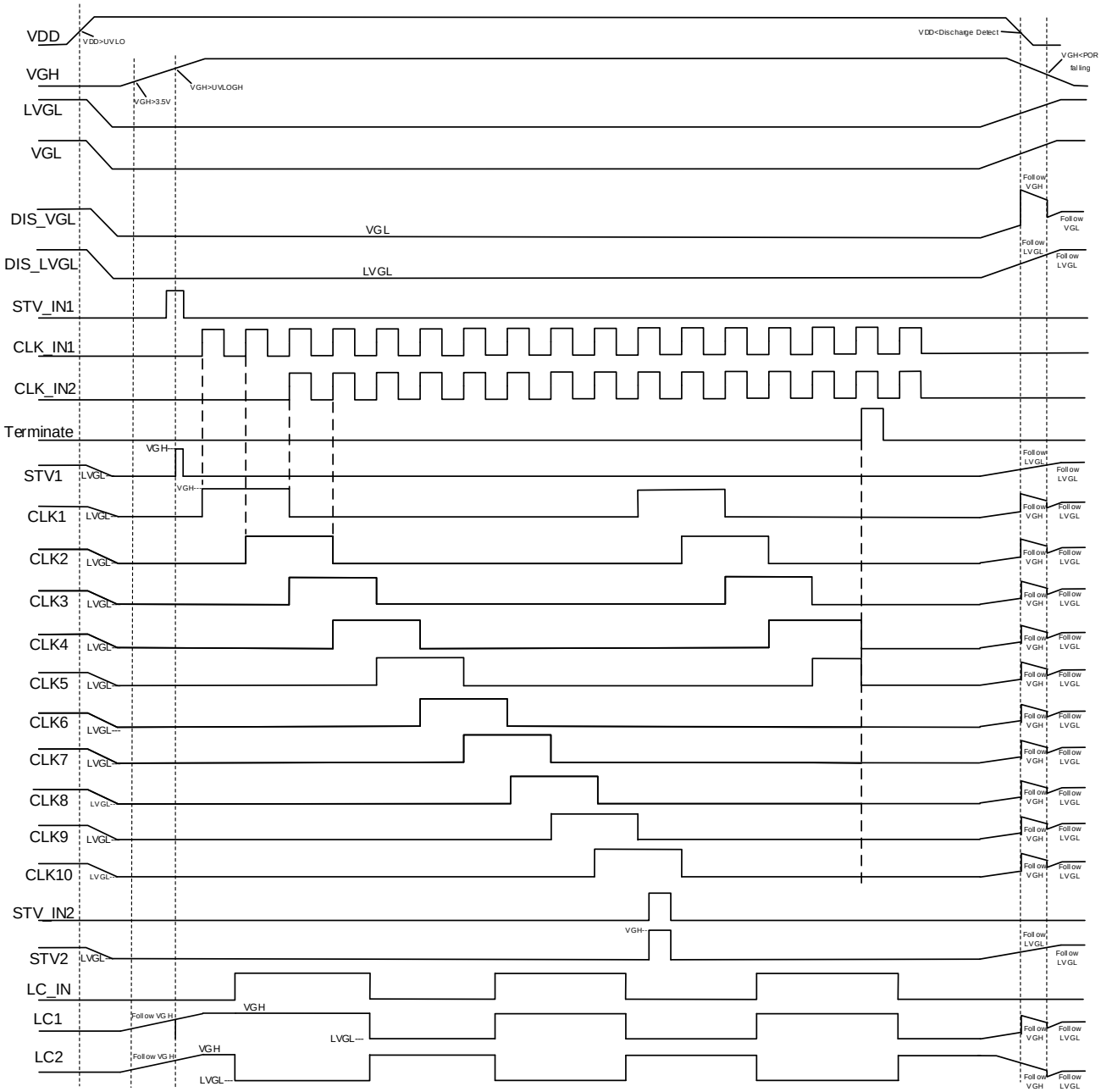


Figure 2-1. The iML7272A A-si Mode Power Sequence

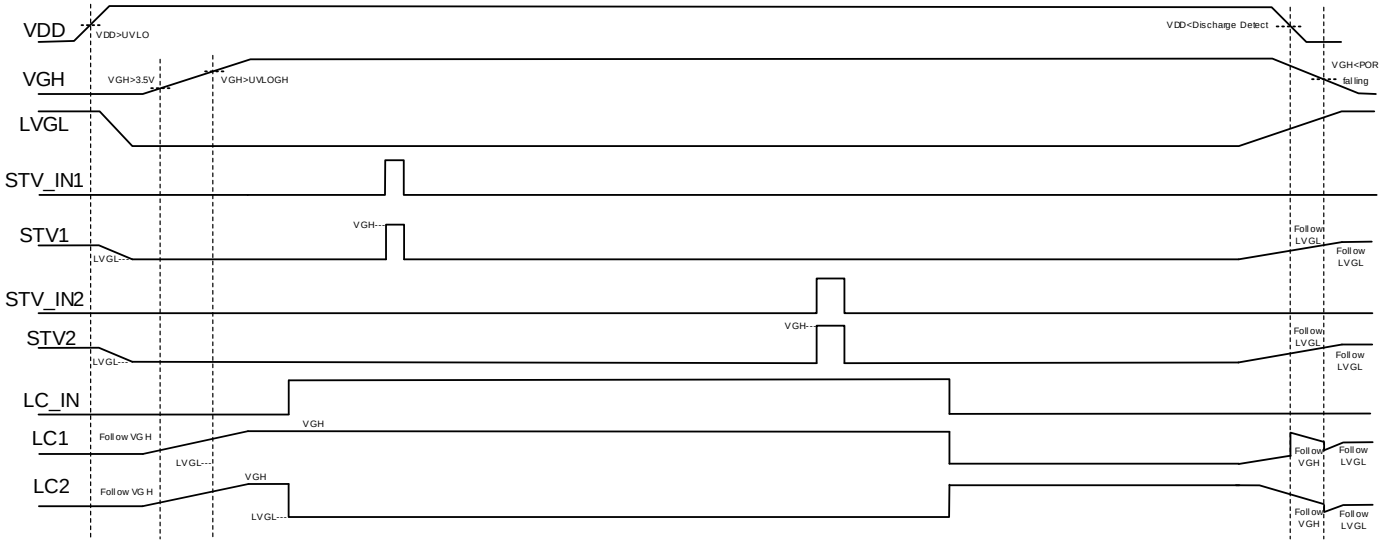


Figure 2-2. The iML7272A A-si Mode (Reg01h[1:0]=00b)

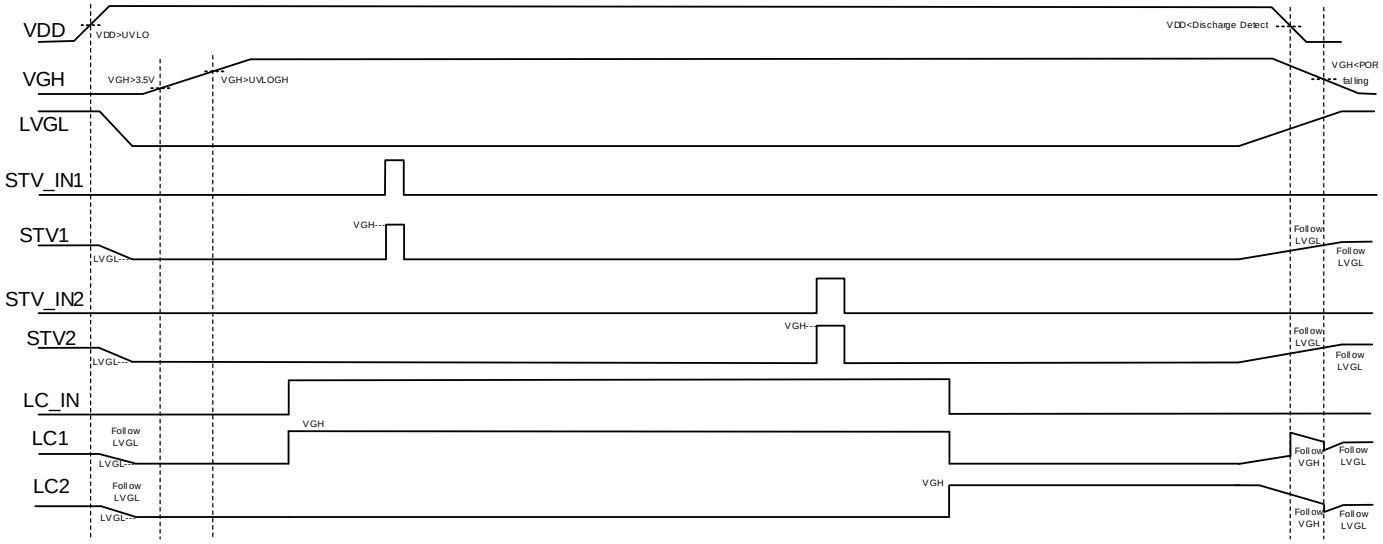


Figure 2-3. The iML7272A IGZO Mode (Reg01h[1:0]=01b)

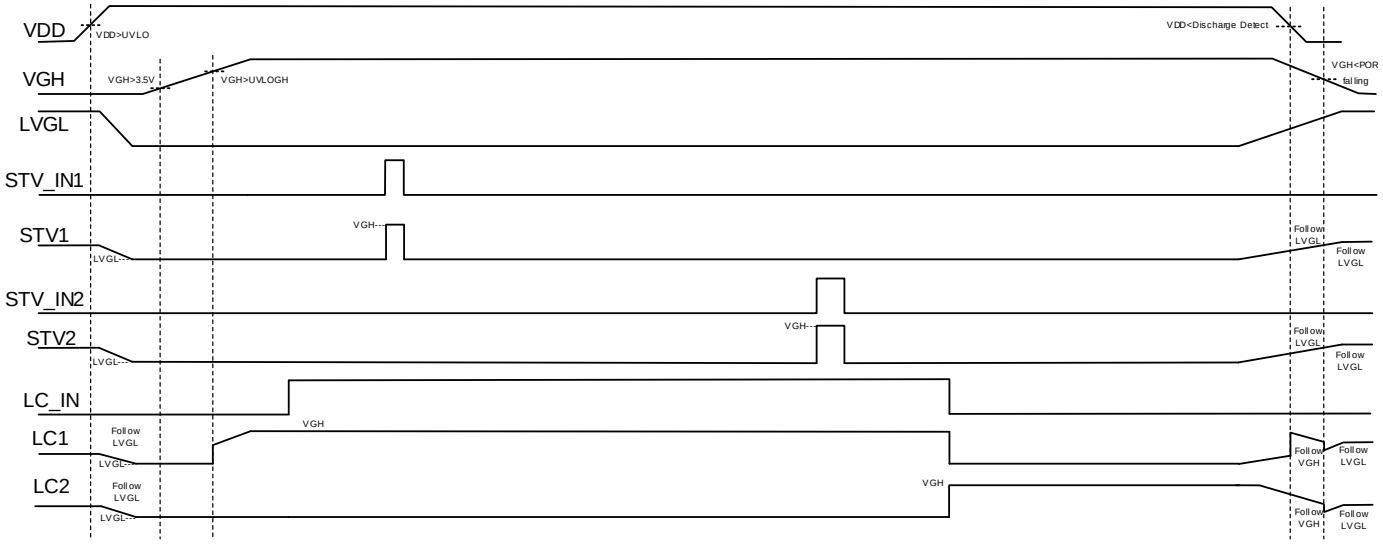


Figure 2-4. The iML7272A IGZO Mode (Reg01h[1:0]=10b)

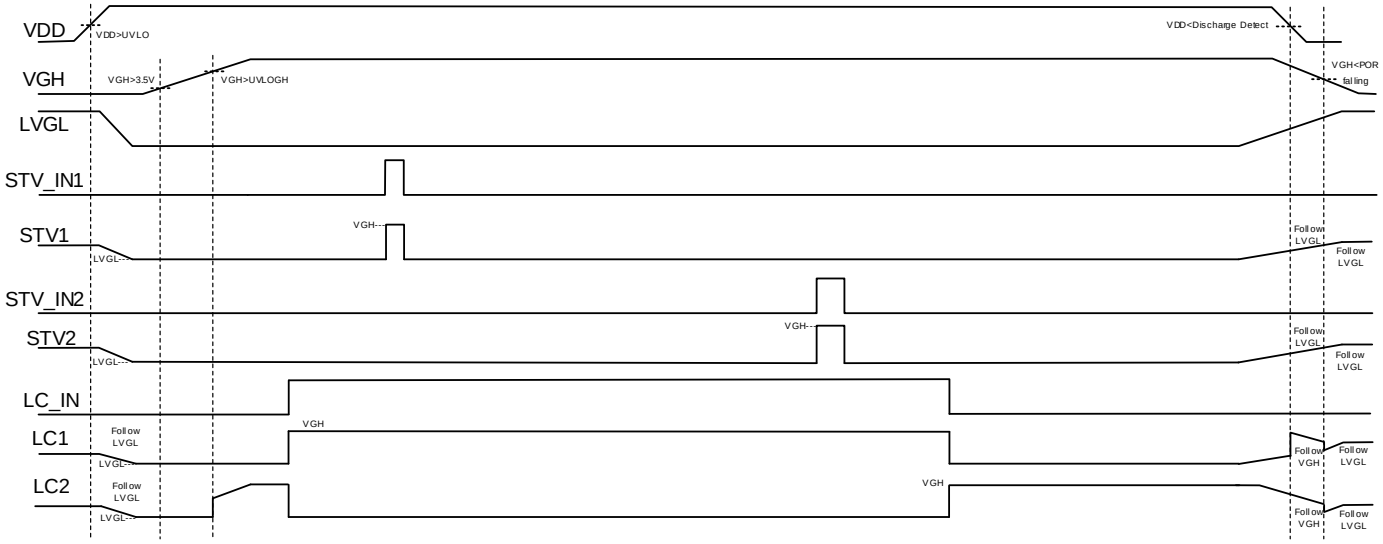


Figure 2-5. The iML7272A IGZO Mode (Reg01h[1:0]=11b)

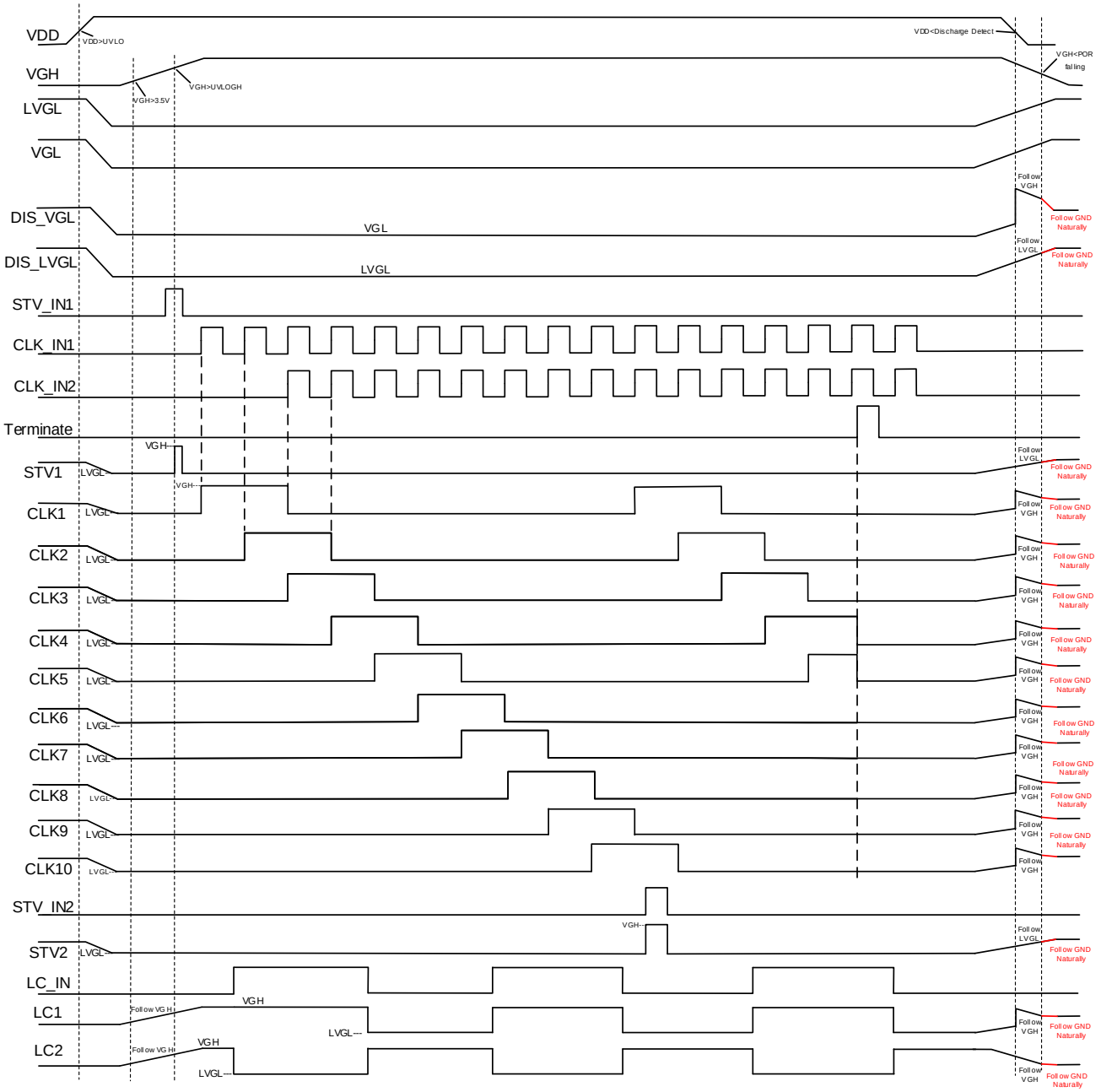


Figure 2-6. The iML7272A IGZO Mode (Reg01h[2]=1b)

Table 1. Power On (from 0 to VDD) Condition

Case	Analog Power Input			Logic Input				Analog Output					
	VDD	DIS_SENSE	VGH	STV_in1	STV_in2	CLK_IN	LC_IN	STV1	STV2	CLK	LC1/LC2	DIS_VGL	DIS_LVGL
1	<UVLO 2.2V	Don't Care	<UVLO 15V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	LVGL	VGL	LVGL
2.1	>UVLO 2.2V	Don't Care	<UVLO 15V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	VGH	VGL	LVGL
2.2	<UVLO 2.2V	Don't Care	>UVLO 15V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	Hi-Z	VGL	LVGL
3	>UVLO 2.2V	<2.5V+Hys	>UVLO 15V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	VGH	VGL	LVGL
4.1	>UVLO 2.2V	>2.5V+Hys	>UVLO 15V	w/o signal	-	w signal	w signal	LVGL	-	LVGL	LC1=LC_IN LC2=LC1_B	VGL	LVGL
4.2	>UVLO 2.2V	>2.5V+Hys	>UVLO 15V	w signal	-	w/o signal	w/o signal	Normal Operation	-	LVGL	VGH	VGL	LVGL
4.3	>UVLO 2.2V	>2.5V+Hys	>UVLO 15V	w signal	-	w signal	w signal	Normal Operation	-	Normal Operation	LC1=LC_IN LC2=LC1_B	VGL	LVGL
4.4	>UVLO 2.2V	>2.5V+Hys	>UVLO 15V	-	w/o signal	-	-	-	LVGL	-	-	VGL	LVGL
4.5	>UVLO 2.2V	>2.5V+Hys	>UVLO 15V	-	w signal	-	-	-	Normal Operation	-	-	VGL	LVGL
5	>UVLO 2.2V	>2.5V+Hys	>UVLO 15V	w signal	w signal	w signal	w signal	Normal Operation	Normal Operation	Normal Operation	LC1=LC_IN LC2=LC1_B	VGL	LVGL

Table 2. Power Off 1/3 (when DIS_SENSE falls first) Condition

Case	Analog Power Input			Logic Input				Analog Output					
	VDD	DIS_SENSE	VGH	STV_in1	STV_in2	CLK_IN	LC_IN	STV1	STV2	CLK	LC1/LC2	DIS_VGL	DIS_LVGL
1.1	>UVLO 2.0V	<2.5	>UVLO 5V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL※1	LVGL※2	LVGL※3	LVGL※3	VGH	LVGL※4
2.1	<UVLO 2.0V	<2.5	<UVLO 5V >POR 3.5V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL※1	LVGL※2	LVGL※3	LVGL※3	VGH	LVGL※4
3.1	<UVLO 2.0V	<2.5	<POR 3.5V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	LVGL	VGL	LVGL
3.2	>UVLO 2.2V	<2.5	>UVLO 15V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL※1	LVGL※2	LVGL※3	LVGL※3	VGH	LVGL※4
2.2	>UVLO 2.2V	>2.5V+Hys	>UVLO 15V	Follow Power On sequence. (Abnormal power off).									
4.1	>UVLO 2.2V	<2.5	<POR 3.5V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	VGH	VGL	LVGL

Table 3. Power Off 2/3 (when VGH falls first) Condition

Case	Analog Power Input			Logic Input				Analog Output					
	VDD	DIS_SENSE	VGH	STV_in1	STV_in2	CLK_IN	LC_IN	STV1	STV2	CLK	LC1/LC2	DIS_VGL	DIS_LVGL
1.2	>UVLO 2.2V	>2.5+Hys	<UVLO 5V >POR 3.5V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL※1	LVGL※2	LVGL※3	LVGL※3	VGH	LVGL※4
2.1	<UVLO 2.0V	<2.5	<UVLO 5V >POR 3.5V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL※1	LVGL※2	LVGL※3	LVGL※3	VGH	LVGL※4
3.1	<UVLO 2.0V	<2.5	<POR 3.5V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	LVGL	VGL	LVGL
2.2	>UVLO 2.2V	>2.5+Hys	>UVLO 15V	Follow Power On sequence. (Abnormal power off).									
2.4	>UVLO 2.2V	>2.5+Hys	<POR 3.5V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	VGH	VGL	LVGL

Table 4. Power Off 3/3 (when VDD falls first) Condition

Case	Analog Power Input			Logic Input				Analog Output					
	VDD	DIS_SENSE	VGH	STV_in1	STV_in2	CLK_IN	LC_IN	STV1	STV2	CLK	LC1/LC2	DIS_VGL	DIS_LVGL
1.3	<UVLO 2.0V	>2.5V+Hys	>UVLO 5V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL※1	LVGL※2	LVGL※3	LVGL※3	VGH	LVGL※4
2.5	<UVLO 2.0V	Don't Care	<UVLO 5V >POR 3.5V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL※1	LVGL※2	LVGL※3	LVGL※3	VGH	LVGL※4
3.3	<UVLO 2.0V	Don't Care	<POR 3.5V	Don't Care	Don't Care	Don't Care	Don't Care	LVGL	LVGL	LVGL	LVGL	VGL	LVGL
2.2	>UVLO 2.2V	>2.5V+Hys	>UVLO 15V	Follow Power On sequence. (Abnormal power off).									

Notes:

(1) ※1 : For STV1 Discharge state. Select LVGL or VGH by 04h[3]
(2) ※2 : For STV2 Discharge state. Select LVGL or VGH by 04h[4]
(3) ※3 : For CLKx and LCx Discharge state. Select LVGL or VGH by 04h[6]
(4) ※4 : For DIS_LVL Discharge state. Select LVGL or VGH by 04h[5]

THEORY OF OPERATION

General Description

The iML7272A provides 16-channel Level Shifter designed to drive the GOA panel. This device converts the logic-level signals generated by the Timing Controller (TCON) to high-level signals required by GOA panel.

Power On Sequence

When the VDD exceeds UVLO, the internal signal ENA for condensed GOA logic will be high. The outputs of Level Shifter CLK1~CLK10 and DIS_LVGL should follow LVGL level since VDD exceeds UVLO. The outputs of Level Shifter STV should follow LVGL level since VDD exceeds UVLO. The outputs of Level Shifter LC1 and LC2 should follow LC_IN transient one VGH the other LVGL since VDD exceeds UVLO. After ENA high, CLK1 to CLK10 do not output until receiving the first STV_IN rising edge. After ENA high, LC1 and LC2 will follow LC truth table transient.

LC Truth Table		
LC_IN (from TCON)	0	1
LC1	0	1
LC2	1	0

According to GOA circuit experience, it is recommended that
1. LC1 and LC2 start to work earlier than the 1st STV_IN by 2us;
2. Logic signal (STV_IN, LC_IN, CLK_IN1 to 2) must be sent after VGH power ready.
The recommended power-on sequence is VDD (2.6 to 5.5V) → LVGL → VGL → VGH or VDD (2.6 to 5.5V) → LVGL=VGL → VGH. The most negative voltage LVGL must be ready before the other negative voltage VGL.

Power Off Sequence

Once the VDD falls below the UVLO threshold, the iML7272A will have the following actions.
Pulling all level-shifter outputs as high level or low level according to Reg 04h (Including STV, DIS_LVGL, LC1 to 2, and CLK1 to CLK10).

Protection

The iML7272A contains Over-Temperature Protection (OTP), Over-Current Protection (OCP). The following table shows the main behavior of each protection.

Table 5. Over temperature Protection and Over Current Protections

Function / Protection	Output	FAULT	Recovery
OTP	Hi-Z	Pull low	T_J decrease 20°C(Typ.)
OCP	Hi-Z	Pull low	(VDD < VUVLO) & [V_{GH} < POR falling]

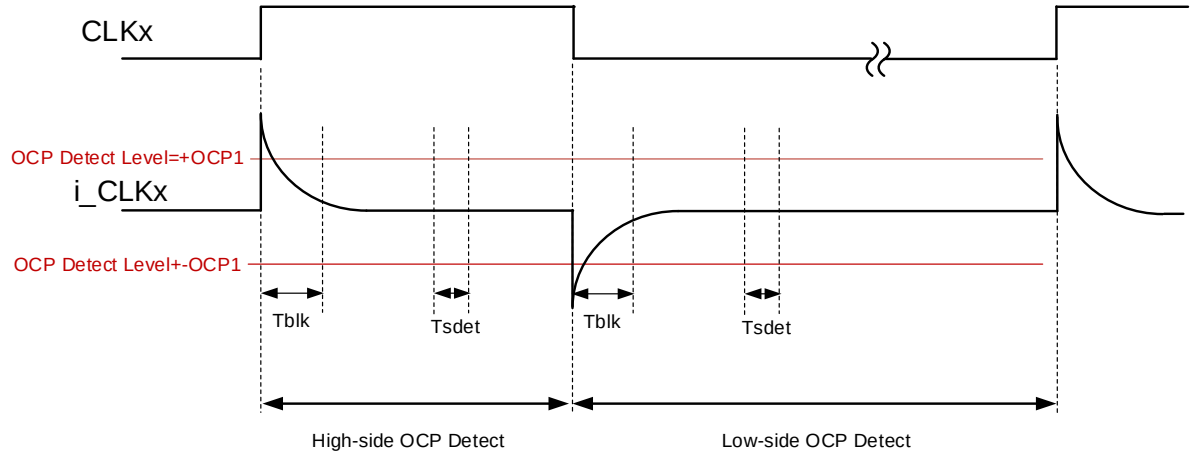
Over-Temperature Protection (OTP)

An Over-Temperature Protection (OTP) is equipped to prevent iML7272A from overheating due to the excessive power dissipation. The OTP will stop operating while junction temperature exceeds 150°C (Min.). All of output channel start operating while the decrease of junction temperature approximately 20°C (Typ.).

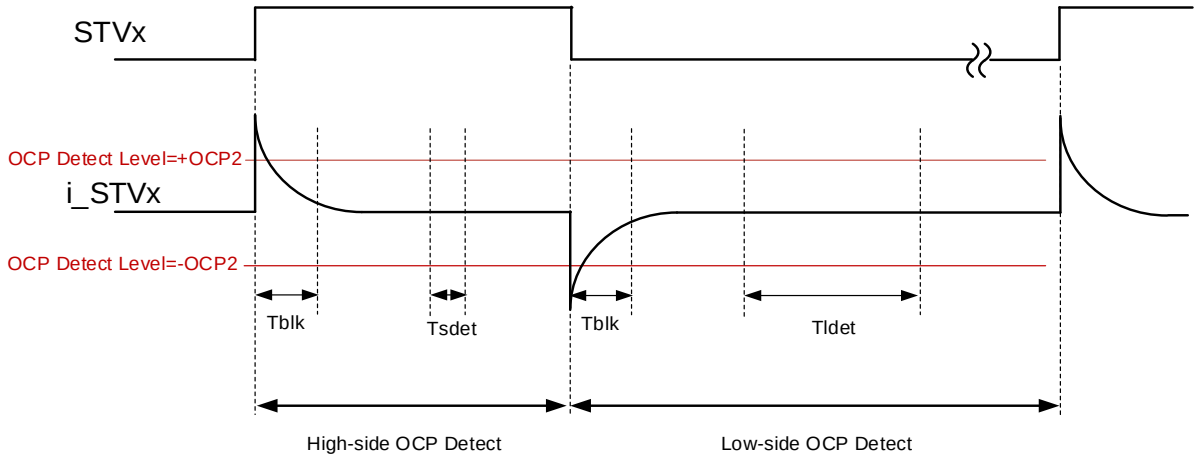
Over-Current Protection (OCP)

The iML7272A can detect output pins (STV, CLK1 to 10, LC1 to 2, DIS_LVGL) if OCP condition happens. If OCP condition happens, the IC all outputs (STV, CLK1 to 10, LC1 to 2, DIS_LVGL) will pull high impendence state. After VUVLO and VGH <POR falling, IC recovers again.

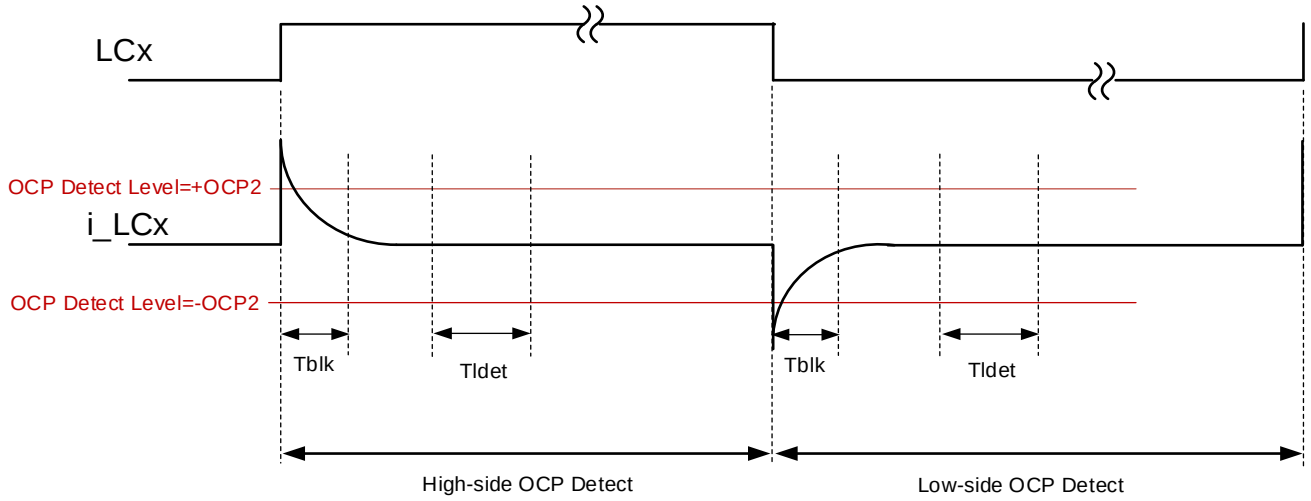
OCP Timing for CLK1 ~ CLK10



OCP Timing for STV1/2



OCP Timing for LC1/2



OCP Timing for DIS_LVGL/VGL

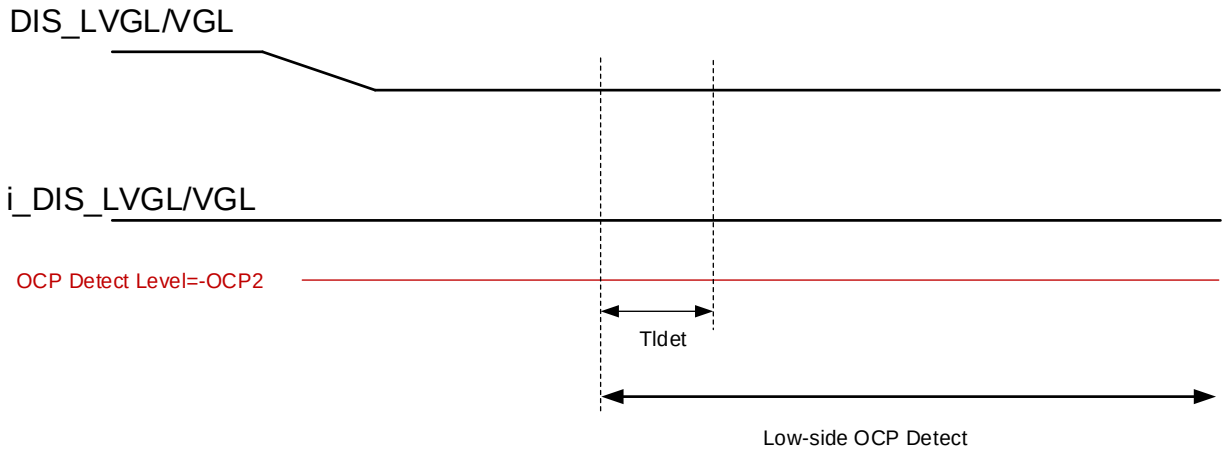


Figure 3. OCP Detection Waveforms

IC FAULT Function

During normal operating, FAULT pin becomes high-state. OTP or OCP happen, the FAULT pin becomes low-state and and each output channel follows high impedance state.

Timing Diagram

REG04H[1:0]=00(4 Phase), REG04H[7]=0(1-Line Mode)

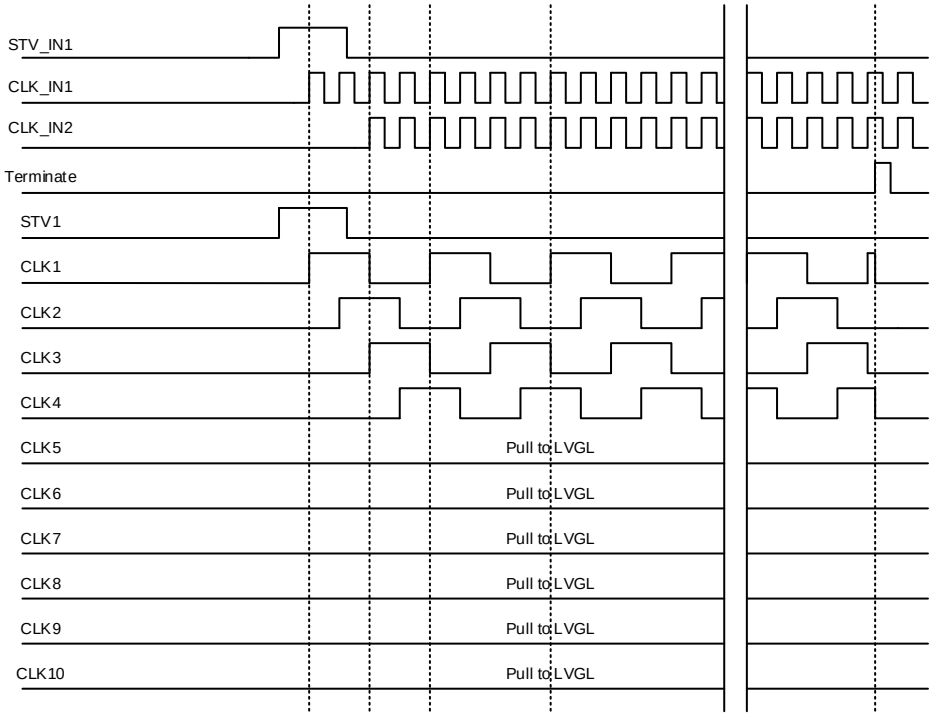


Figure 4. 2-In 4-Out 1-Line Mode waveforms (CLK5 to 10 still do discharge at power-off)

REG04H[1:0]=00(4 Phase), REG04H[7]=1(2-Line Mode)

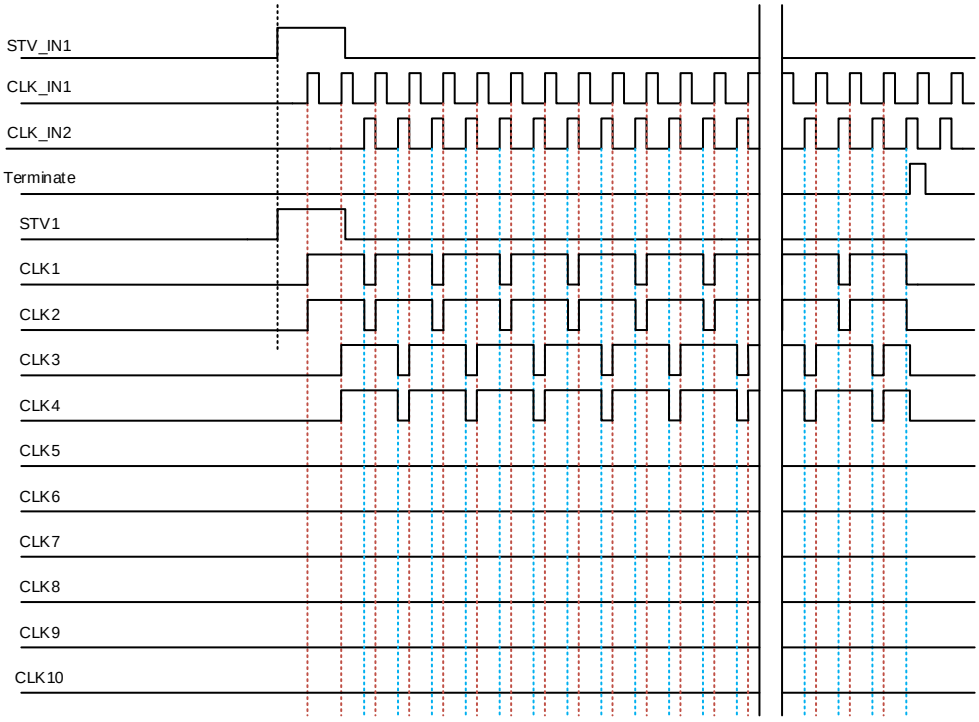


Figure 5. 2-In 4-Out 2-Line Mode waveforms (CLK5 to 10 still do discharge at power-off)

REG04H[1:0]=01(6 Phase), REG04H[7]=0(1-Line Mode)

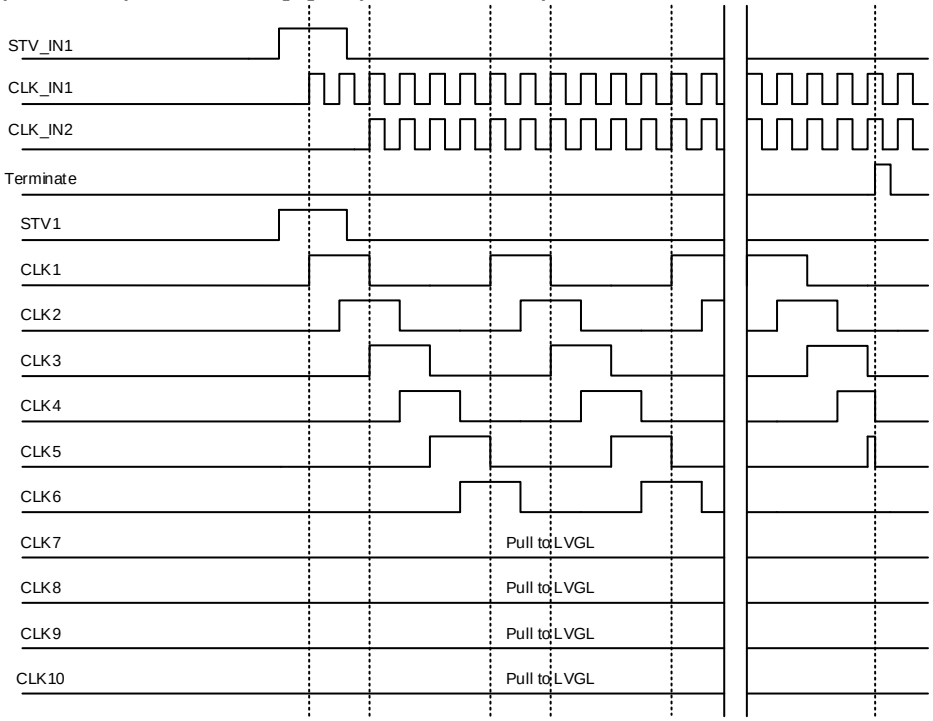


Figure 6. 2-In 6-Out 1-Line Mode waveforms (CLK7 to 10 discharge at power-off)

REG04H[1:0]=01(6 Phase), REG04H[7]=1(2-Line Mode)

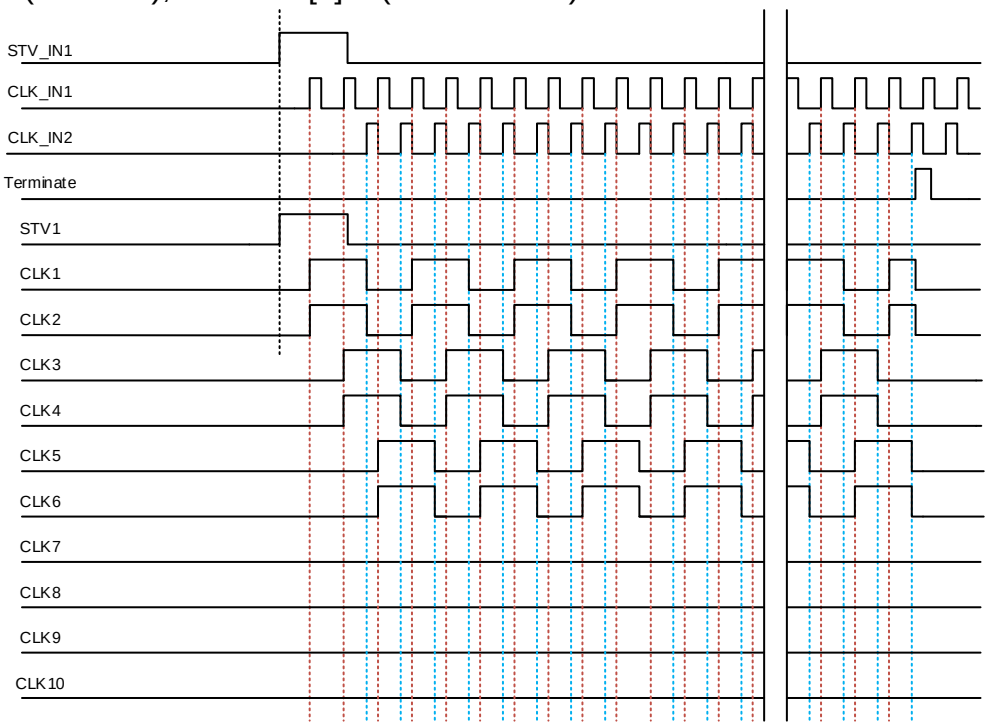


Figure 7. 2-In 6-Out 2-Line Mode waveforms (CLK7 to 10 discharge at power-off)

REG04H[1:0]=10(8 Phase), REG04H[7]=0(1-Line Mode)

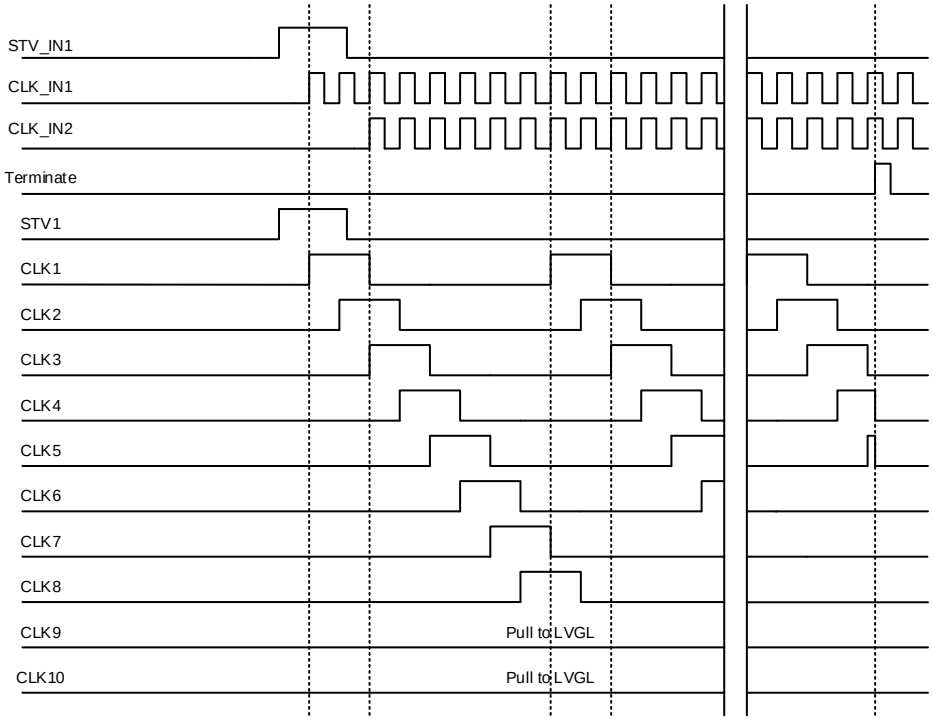


Figure 8. 2-In 8-Out 1-Line Mode waveforms (CLK9 to 10 discharge at power-off)

REG04H[1:0]=10(8 Phase), REG04H[7]=1(2-Line Mode)

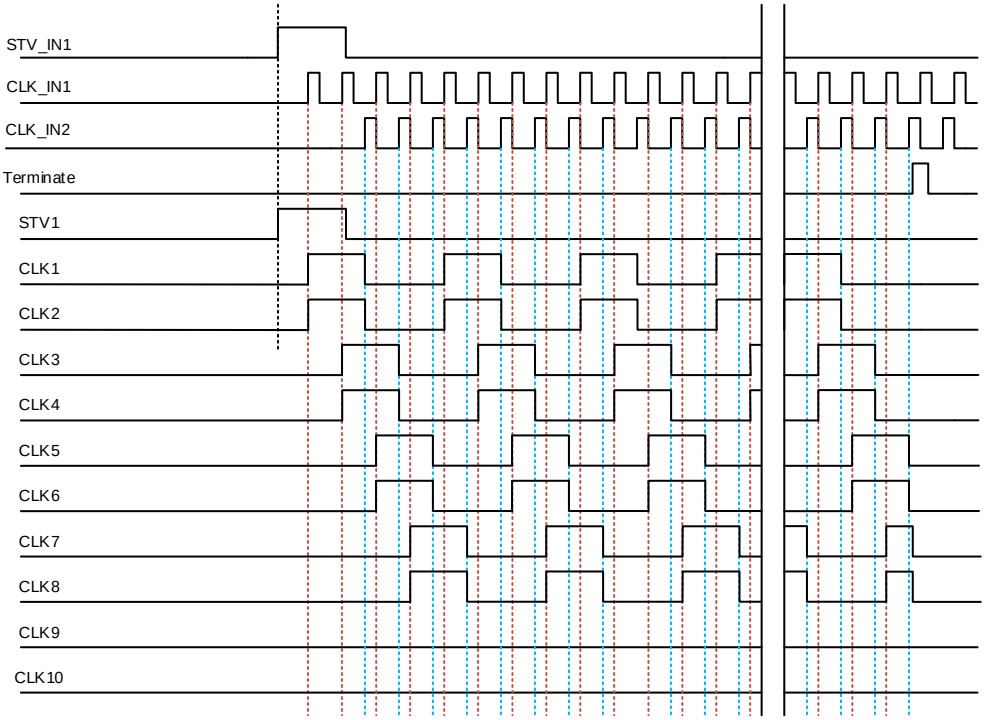


Figure 9. 2-In 8-Out 2-Line Mode waveforms (CLK9 to 10 discharge at power-off)

REG04H[1:0]=11(10 Phase), REG04H[7]=0(1-Line Mode)

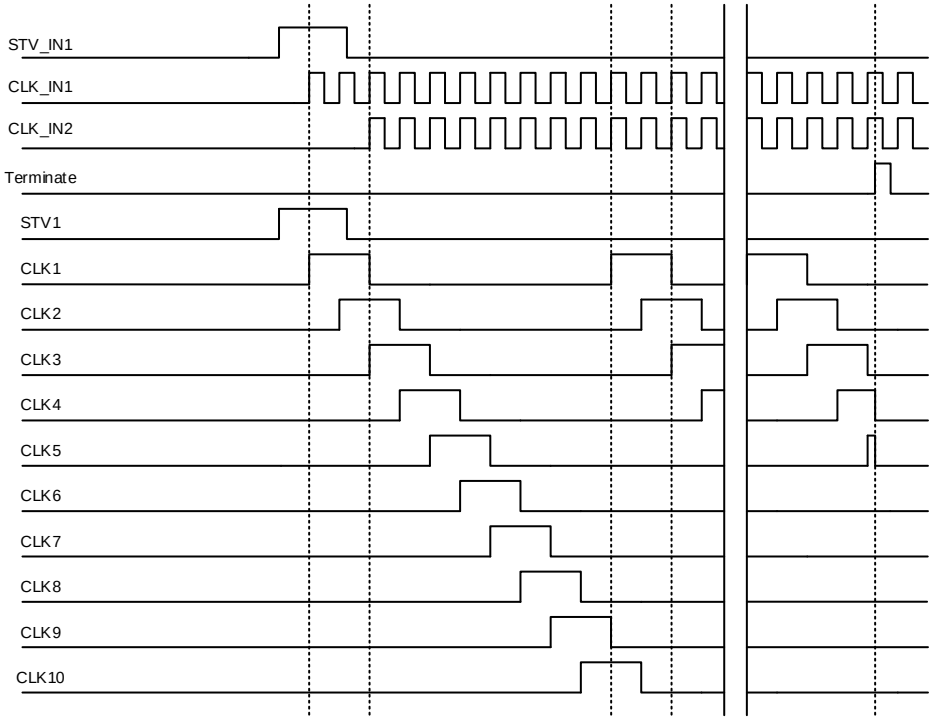


Figure 10. 2-In 10-Out 1-Line Mode waveforms

REG04H[1:0]=11(10 Phase), REG04H[7]=1(2-Line Mode)

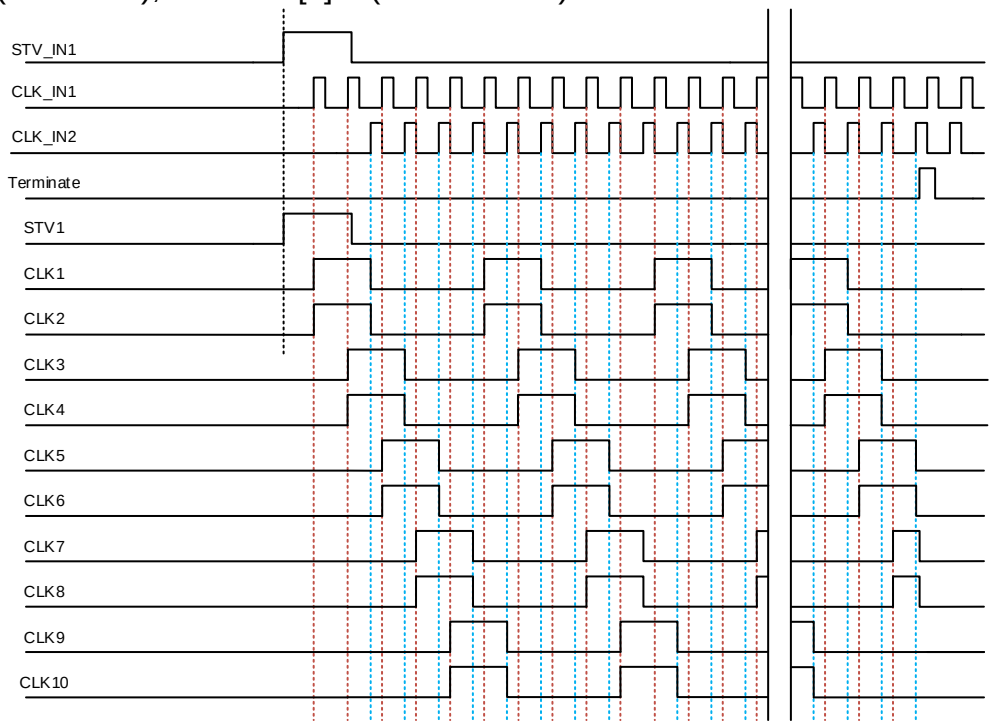


Figure 11. 2-In 10-Out 2-Line Mode waveforms

I²C Serial Interface

The iML7272A uses two wires, serial data (SDA) and serial clock (SCL), to communicate. They are connected via the resistors to an external positive power supply voltage. This means that when the bus is free, both lines are high. The device on the bus has open-drain pins. Each device on the I²C bus responds to a slave address byte sent immediately following a Start Condition. Figure 8 shows the definition of timing on I²C bus.

The slave address byte contains the slave address in the most significant 7 bits and the R/W bit in the least significant bit. The iML7272A consist of slave address. Table 6 shows the slave address.

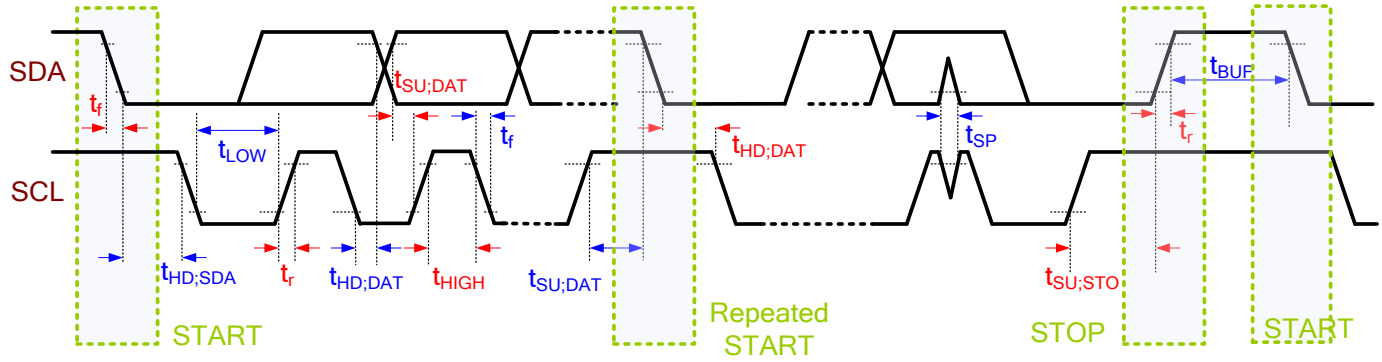


Figure 12. Timing on I²C bus

Table 6. Slave Address byte

Bit	MSB	6	5	4	3	2	1	LSB
Data	0	1	0	1	0	0	A0	R / $\overline{W}$

Memory of the iML7272A

The iML7272A has two types of memory. One type is non-volatile NVM and the other is volatile register memory. The NVM stores all register code values for the iML7272A even when the chip is not powered. When the chip is powered up, all code values of the NVM are automatically copied into the volatile register memory. The volatile register memory can be written or read through I²C at any time.

Write/Read Data to/from the iML7272A

Write operation One 8-bit data value is written into the register by each I²C WRITE operation.
A write to the iML7272A consists of START condition, the slave address of iML7272A with R/W bit set to 0, the memory address, 8bits of data, and STOP condition.
A special command code, writing Reg00h=A5h by I²C WRITE operation, makes writing all register code data into the internal NVM. A special command code, writing Reg00h=A4h by I²C WRITE operation, makes all NVM data downloaded to the register. X is decided by A0 pin.

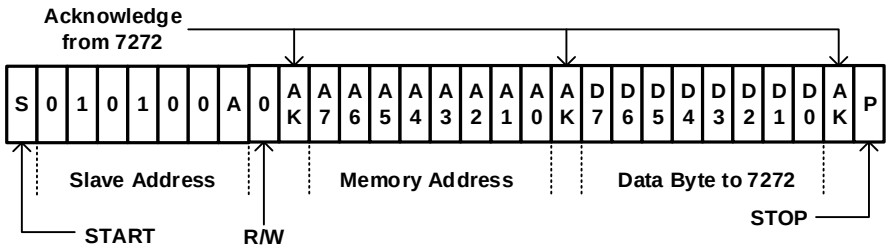


Figure 13. Writing a byte of data

Read operation One 8-bit data value is read from the register by each I²C READ operation. The stored data on the NVM is not directly accessible during a normal read operation. All NVM data is copied into register memory whenever the power is newly on, or the special command of Reg00h=A4h by I²C. If another 8-bits of data needs to be read, a new memory address must be written by a new I²C READ operation. Consecutive data reads without writing a memory address is not allowed.

A read from the iML7272A consists of START condition, the slave address of iML7272A with R/W bit set to 0, the memory address, repeated START condition, and the slave address of iML7272A with R/W bit set to 1. Then the iML7272A transmits the contents of the register memory. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). A STOP condition can be issued after reading one data byte.

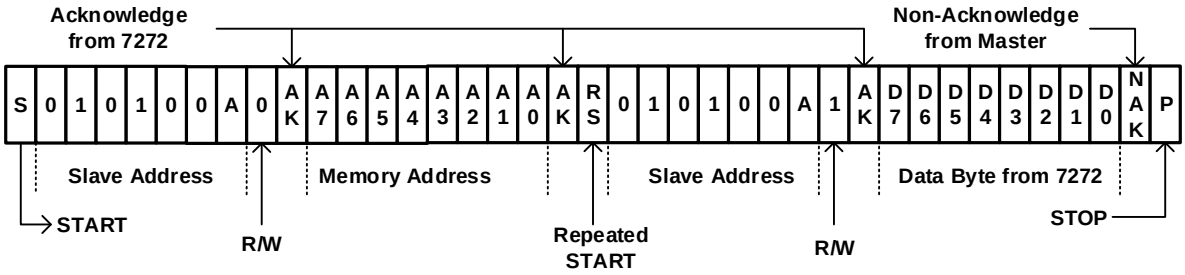


Figure 14. Reading a byte of data

Register Map

Reg	Name	Description	Default Value	Range	Note
00h	Control Byte (write only)	0x00 = A5 → WR Register Data to NVM (0x02h to 0x04h) 0x00 = A4 → Download NVM to Regsister (0x02h to 0x04h)	-	-	Write only Register (Non NVM)
01h	LC_Power ON_SET	[1:0] LC_Power ON_SET	00b	00b: LC1/LC2 follow VGH 01b: LC1/LC2 follow LVGL 10b: LC1 follow VGH, LC2 follow LVGL 11b: LC1 follow LVGL, LC2 follow VGH	
	Power_off_ POR	[2]	0b	0b: Follow LVGL 1b: Follow GND Naturally	
02h	CLK_OCP_ LEVEL	[2:0] CLK_OCP_LEVEL	100b: 90mA	000b: Disable 001b: 30mA 010b: 50mA 011b: 70mA 100b: 90mA 101b: 120mA 110b: 160mA 111b: 200mA	-
	STV&LC& DIS_OCP_ LEVEL	[5:3] STV&LC&DIS_OCP_ LEVEL	100b: 90mA	000b: Disable 001b: 30mA 010b: 50mA 011b: 70mA 100b: 90mA 101b: 120mA 110b: 160mA 111b: 160mA	-
	CLK_OCP_ COUNT	[7:6] CLK_OCP_COUNT	01b: 8 times	00b: 4 times 01b: 8 times 10b: 16 times 11b: 32 times	Continuous Trigger
03h	OCP_ BLK_TIME	[2:0] OCP_BLK_TIME	011b: 8us	000b: 2us 001b: 4us 010b: 6us 011b: 8us 100b: 10us 101b: 12us 110b: 14us 111b: 16us	-
	STV_OCP_ COUNT	[3] STV_OCP_COUNT	0b: 4 times	0b: 4 times 1b: 16 times	Continuous Trigger
	DIS_SENSE Detect	[5:4] DIS_SENSE Detect	01b: 2.5V	00b: 2.3V 01b: 2.5V 10b: 2.7V 11b: 2.9V	-
	CLK Slew Rate	[7:6] CLK Slew Rate	00b: 1000V/us	00b:1000V/us 01b:700V/us 10b:400V/us 11b:100V/us	-
04h	CLK_PH_SE L	[1:0] CLK Phase Select	11b:10 phase	00b: 4 phase 01b: 6 phase 10b: 8 phase 11b: 10 phase	
	SEL_STV1_ RESET	[2] SEL_STV1_RESET	1b: Reset CLKx to LVGL	0b: Don't reset anything 1b: Reset CLKx to LVGL	-
	DIS_STV1_ SEL	[3] DIS_STV1_SEL	0b: Pull to LVGL	0b: Pull to LVGL 1b: Pull to VGH	-
	DIS_STV2_ SEL	[4] DIS_STV2_SEL	0b: Pull to LVGL	0b: Pull to LVGL 1b: Pull to VGH	
	DIS_LVGL_ SEL	[5] DIS_LVGL_SEL	0b: Pull to LVGL	0b: Pull to LVGL 1b: Pull to VGH	-
	DIS_CLK_L C_SEL	[6] DIS_CLK_LC_SEL	1b: Pull to VGH	0b: Pull to LVGL 1b: Pull to VGH	-
	CLK_Mode_ SEL	[7] CLK_Mode_SEL	0b: 1-Line	0b: 1-Line 1b:2-Line	-

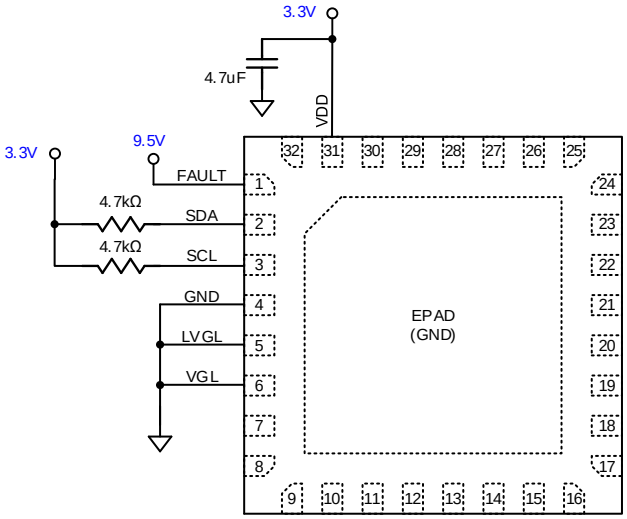
Register Details

Control register Set (0x00)

The Non-Volatile Memory (NVM) will be written to or read from via the Control Register.
The control register is a register only (cannot be written into NVM)

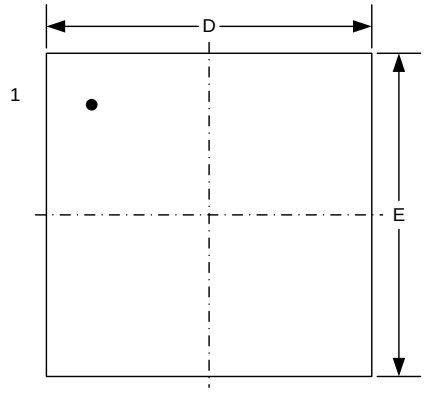
Name	Bit	Access	Default	Description
Control Reg 0x00	7	W	0	0x00 = A5 → WR Register Data to NVM (0x02h to 0x04h) 0x00 = A4 → Download NVM to Register (0x02h to 0x04h)
	6		0	
	5		0	
	4		0	
	3		0	
	2		0	
	1		0	
	0		0	

Power Rail of Programming NVM

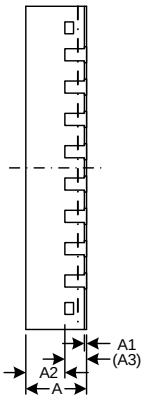


PACKAGE INFORMATION

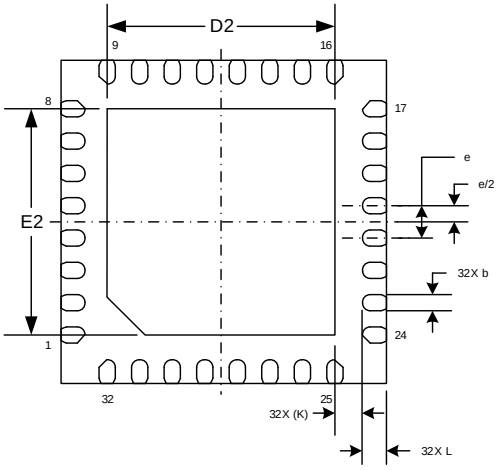
QFNWB4x4-32L



TOP VIEW



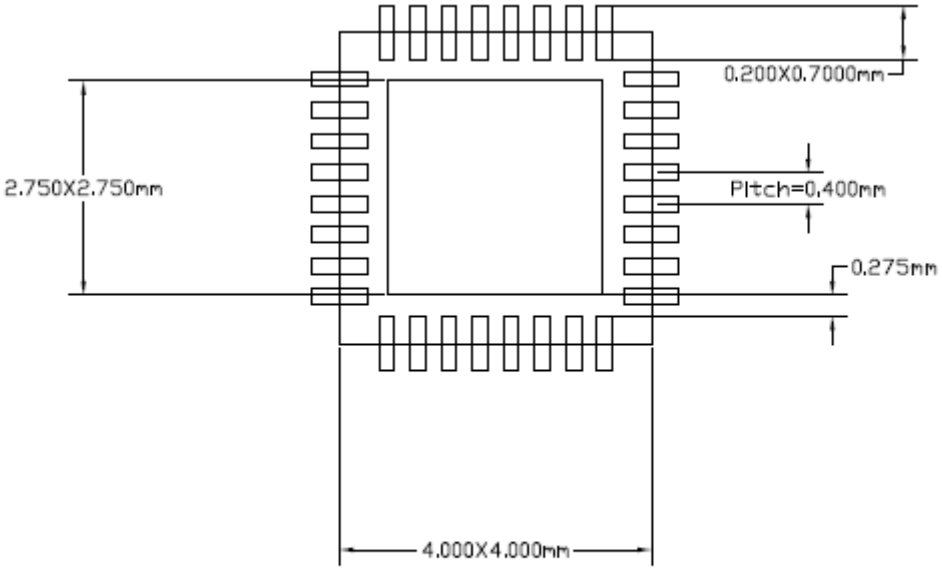
SIDE VIEW



BOTTOM VIEW

		Symbol	Min	Nom	Max
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0.00	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F WIDTH		A3		0.20 REF	
LEAD WIDTH		b	0.15	0.20	0.25
BODY SIZE	X	D		4.00 REF	
	Y	E		4.00 REF	
LEAD PITCH		e		0.40 BSC	
EP SIZE	X	D2	2.60	2.75	2.90
	Y	E2	2.60	2.75	2.90
LEAD LENGTH		L	0.20	0.35	0.50
LEAD TIP TO EXPOSED PAD EDGE		K		0.30 REF	

LAND PATERN FOR QFNWB4x4-32L PACKAGE



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